Claims

We claim:

1. A self-noise cancellation mechanism for reducing performance degradation as a result of self-generated noise, comprising:

a pulse-forming network for producing an internally-generated UWB bi-phase signal having a first arranged pattern;

a mixer for combining the UWB bi-phase signals with an incoming RF UWB signal having a second set pattern; and

an integrator for accumulating an output of the mixer,

wherein the first arranged pattern comprises a first set of bi-phase wavelets and an adjacent second set of bi-phase wavelets,

wherein the second arranged pattern comprises a third set of bi-phase wavelets and an adjacent fourth set of bi-phase wavelets,

wherein the first set of bi-phase wavelets and the third set of bi-phase wavelets are the same in wave shape and polarity, and

wherein the second set of bi-phase wavelets and the fourth set of bi-phase wavelets are the same in wave shape, but are inverted in polarity.

2. A self-noise cancellation mechanism as recited in claim 1, wherein the first and third sets of bi-phase wavelets each comprise two wavelets.

3. A UWB self-noise cancellation mechanism as recited in claim 1, wherein the second and third sets of bi-phase wavelets each comprise two wavelets.

4. A self-noise cancellation mechanism as recited in claim 1, wherein the first, second, third, and fourth sets of bi-phase wavelets all have equal number of wavelets.

5. A self-noise cancellation mechanism as recited in claim 1, further comprising an antenna for receiving the incoming RF UWB signal.

6. A self-noise cancellation mechanism as recited in claim 5, further comprising a front end circuit located between the antenna and the mixer for processing the incoming RF UWB signal.

7. A self-noise cancellation mechanism as recited in claim 6, wherein the front end circuit includes one of a low noise amplifier, an automatic gain control circuit, and a stub circuit.

8. A self-noise cancellation mechanism as recited in claim 1, further comprising an analog-to-digital converter for converting the output of the integrator into a digital signal.

9. A self-noise cancellation mechanism in a radio receiver, comprising:

means for producing an internally-generated UWB bi-phase signal having a first arranged pattern;

means for receiving an incoming RF signal having a second arranged pattern;

means for combining the internally-generated UWB bi-phase signal and the incoming RF signal to produce an output; and

means for integrating the output of the combining means over a length of time that corresponds with the first and second arranged patterns such that an integration output approaches zero when the incoming RF signal is aligned in phase with the internally-generated UWB bi-phase signal.

10. A mode selection mechanism, comprising:

a clock signal generator for generating a base clock signal at a base clock frequency;

a first divide circuit for dividing the base clock signal by a first integer value M to generate a first clock signal having a first clock frequency equal to the base clock frequency divided by M;

a second divide circuit for dividing the base clock signal by a second integer value N to generate a second clock signal having a second clock frequency equal to the base clock frequency divided by N; and

a switch for selecting the first clock signal when a first receive mode of operation is selected, and for selecting the second clock signal when a second receive mode of operation is selected.

11. A mode selection mechanism, as recited in claim 10, wherein the first receive mode is a UWB receive mode.

12. A mode selection mechanism as recited in claim 10, wherein the base clock frequency is about 4.8 GHz.

13. A mode selection mechanism as recited in claim 12, wherein the first integer value M is equal to 3, and the second integer value N is equal to 2.

14. A mode selection mechanism in a multi-mode radio receiver, comprising:

a mode selector for selecting a receive mode of operation for a received signal;

an agile clock for providing a base clock signal at a base clock frequency;

a frequency divider means for dividing the frequency of the base clock frequency by an integer corresponding to the selected receive mode to generate a divided clock signal having a divided clock frequency; and

a signal processor for processing the received signal with the divided clock signal.

15. A mode selection mechanism in a multi-mode radio receiver, as recited in claim 14, wherein the selected receive mode of operation is a UWB mode.

16. A mode selection mechanism in a multi-mode radio receiver, as recited in claim 14, wherein the frequency divider further comprises:

a first frequency dividing unit, corresponding to a first receive mode, for dividing the frequency of the base clock frequency by a first integer to generate a first divided clock signal having a first divided clock frequency; and

a second frequency dividing unit, corresponding to a second receive mode, for dividing the frequency of the base clock frequency by a second integer to generate a second divided clock signal having a second divided clock frequency.

17. A mode selection mechanism in a multi-mode radio receiver, as recited in claim 16, wherein the first integer is 2 and the second integer is 3.

18. A mode selection mechanism in a multi-mode radio receiver, comprising:

means for selecting a receive mode of operation;

means for providing a base clock signal at a base clock frequency;

means for dividing the frequency of the base clock frequency by an integer corresponding to the selected receive mode to generate a divided clock signal having a divided clock frequency; and

means for processing a received signal with the divided clock signal.

19. A mode selection mechanism in a multi-mode radio receiver, as recited in claim 18, wherein the selected receive mode of operation is a UWB mode.

20. A multi-mode radio receiver, comprising:

a mode selection mechanism including

an agile clock for producing a base clock signal at a base clock frequency,

a first divide circuit for dividing the base clock signal by a first integer to generate a first divided clock signal at a first divided clock frequency,

a second divide circuit for dividing the base clock signal by a second integer to generate a second divided clock signal at a second divided clock frequency, and

a switch for providing a selected clock signal, the selected clock signal being the first divided clock signal when a first receive mode of operation is selected,

and the second divided clock signal when a second receive mode of operation is selected; and

a UWB self-noise cancellation mechanism including

a pulse forming network for producing a series of UWB bi-phase signals based on the selected clock signal,

a mixer for combining the series of UWB bi-phase signals with an incoming RF signal, and

an integrator configured to accumulate an output of the mixer.

21. A multi-mode radio receiver, as recited in claim 20, wherein the first integer is 2 and the second integer is 3.

22. A mode selection mechanism in a multi-mode radio receiver, as recited in claim 20, wherein the first receive mode of operation is a UWB mode.

23. A method of operating a multi-mode radio receiver, comprising:

generating a base clock signal at a base clock frequency;

dividing the base clock signal by a first integer to generate a first divided clock signal at a first divided clock frequency if a first receive mode is determined; and

dividing the base clock signal by a second integer to generate a second divided clock signal at a second divided clock frequency if a second receive mode is determined.

24. A method of operating a multi-mode radio receiver, as recited in claim 23,

wherein the first integer is 2 and the second integer is 3.

25. A method of operating a multi-mode radio receiver, as recited in claim 23, wherein the first receive mode of operation is a UWB mode.